IN THE SPECIFICATION:

Please amend paragraph **[0003]** as follows:

[0003] In general, the circuits on a chip or die terminate in conductive bond pads arrayed on the die's active surface, typically in one or more rows about the die periphery or across a central portion of the die. These bond pads are generally formed of aluminum or an aluminum alloy and are designed to be conductively connected to terminals of a carrier substrate such as an interposer or circuit board, the pattern of terminals on which may not correspond to the locations of the corresponding bond pads on the die. In addition, the lateral bond ~~pad-to-bond~~ pad-to-bond pad separation (pitch) may be too close for satisfactory direct attachment to a substrate. Thus, if the conductive connection to carrier substrate terminals is to be at least in part by wire bonding, as in a dense wafer-level chip-scale package, it is difficult to achieve the desired connection without crossing of wires, undue closeness of wires, or an overly steep bonding angle, all of which may lead to a higher frequency of shorting, such as may be induced by wire sweep. Currently proposed packages have even greater numbers of bond pads packed into smaller spaces, i.e., with finer pitch.

Please amend paragraph **[0020]** as follows:

[0020] In various exemplary embodiments of the present invention, methods are presented for fabricating semiconductor dice in a configuration which may facilitate forming semiconductor die assemblies of improved reliability with greater ease and economy. More particularly, the methods of the present invention avoid the use of one or more redistribution metallization layers for connecting die bond pads to an array of conductive bumps. The invention applies not only to assemblies including one or more dice, such as chip-scale ~~wire-bonded~~ wire-bonded packages and flip-chip packages, but may also be employed in fabricating other semiconductor die packages and assemblies.

Please amend paragraph **[0024]** as follows:

[0024] The present invention also encompasses, in additional embodiments, semiconductor die assemblies and packages fabricated of the present invention as well as ~~higher-level~~ higher-level assemblies incorporating the present invention.

Please amend paragraph **[0048]** as follows:

[0048] The next act 82 utilizes application of an anisotropically conductive material 60, such as a commercially available film or tape illustrated in FIG. 5, to die 50. Such anisotropically conductive materials 60 are also known in the industry as z-axis tape or z-axis film and are electrically conductive in only one direction, i.e., parallel to the z-axis or vertical axis, perpendicular to the plane of the film or tape. As shown, one type of anisotropically conductive material 60 may comprise a film or tape of insulative polymer 76 of a height or thickness 72, into which a relatively dense pattern of parallel conductive metal elements 74 is embedded, generally passing through the film or tape from an upper surface 75 to a backside 77 thereof. The insulative polymer 76 is typically a dielectric material such as polyimide or other polymer. The conductive metal elements 74 may be columns formed of, for example, a metal such as tungsten, aluminum, copper, silver, gold, or alloys thereof and exposed at their upper ends 81, i.e. on the upper surface 75 of the anisotropically conductive material 60, so that conductive bumps or balls may be bonded to the columns. It is currently preferred that the columns 74 be formed of gold. The column diameter 79 may vary but, for example, may be between about 1 μm and about 15 μm. It is currently more preferred that the column diameter 79 be between about 2 μm and about 8 μm. The column diameter 79 and spacing or pitch 73 are preferably imposed so that a plurality of exposed columns 74 will be bonded to a single conductive bump or ball formed or placed thereon. In FIG. 5, the diameter 59 of the footprint of an exemplary conductive bump is shown in broken lines as at least partially contacting a dozen or more columns 74. The exposed column ~~upperends~~ upper ends 81 may occupy only a small portion of the upper tape surface 75 and still effectively retain the conductive bumps or balls by metallurgical bonding thereto. The anisotropically conductive material 60 is shown in FIG. 5

with an adhesive layer 78, such as a pressure-sensitive adhesive layer on the backside 77, for adhesion to a die passivation layer 56 (see FIG. 7).

Please amend paragraph **[0062]** as follows:

[0062] The present invention thus provides a lower cost alternative to the use of conventional redistribution layers and requires fewer process steps with the elimination of ~~under-bump~~ under-bump metallization. Further, the present invention also provides an effective interim solution for wafer-level packaging in which cost is still unacceptably high for low-yielding wafers and conventional wafer-level packaging technology is not yet fully commercialized.